Introduction to DDR2 Memory
Positioning Information (withdrawn product)

Main

Data transfers made to and from a SDRAM DIMM use a synchronous clock signal to establish timing. For example, SDRAM memory transfers data whenever the clock signal makes a transition from a logic low level to a logic high level. Faster clock speeds mean faster data transfer from the DIMM into the memory controller and finally to the processor, or PCI adapters. However, electromagnetic effects induce noise, which limits how fast signals can be cycled across the memory bus.

Double data rate (DDR) memory techniques increase the data rate by transferring data on both the rising edge and the falling edge of the clock signal. DDR DIMMs use a “2x” prefetch scheme so that two sets of 64-bit data are referenced simultaneously. Logic on the DIMM implements multiplexing so that the two 64-bit results (plus ECC bits) appear on each of the rising and falling edges of the clock signal. Thus, two data transfers can be performed during one clock period.

DDR2 is the new generation of DDR technology. The primary benefit is the potential for faster throughput. Currently DDR2 operates at data transfer rates starting at 400 MHz (the upper limit for DDR) and 533 MHz. Support for 667 MHz and 800 MHz transfer rates is expected in 2005.

In addition, the DDR2 improves the power consumption of the DIMM because it works on a lower voltage. DDR operates at a range of 2.5 to 2.8 V, whereas DDR2 only requires 1.8 V. DDR2 consumes less power than DDR and offers a higher range of throughput because it has halved the speed of the memory core (thereby reducing power consumption), but offsetting that by doubling the number of prefetches from the memory core to the I/O buffers (from 2 to 4). This is shown in Figure 1 below.

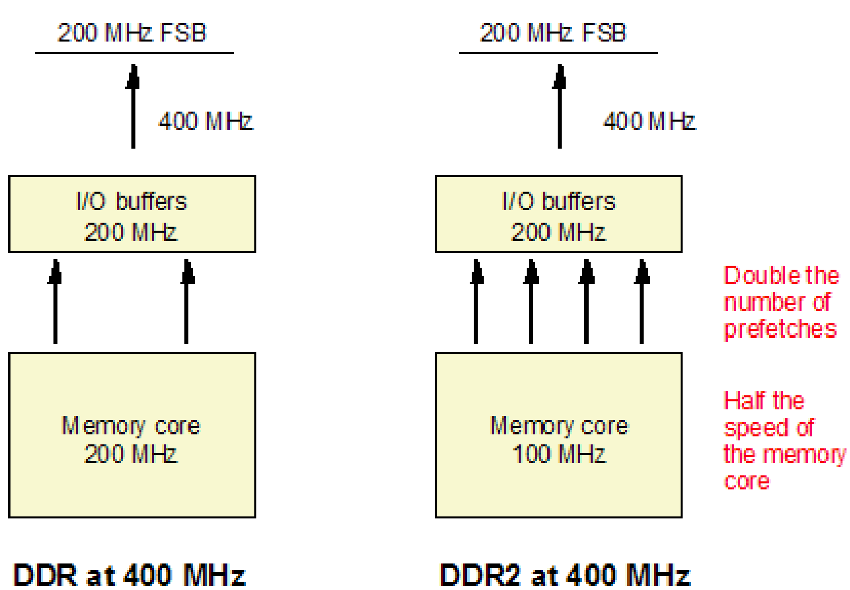

Figure 1: Comparing DDR and DDR2 at the same external frequency

The lower frequency at the memory core means less power consumption and the ability to increase data density (and therefore capacity), and increase speeds as manufacturing technology improves.

The physical pin count of the DIMMs has also changed, meaning that the two standards are not compatible. DDR has 184 pins and DDR2 has 240.

The following table shows the specifications of the current DDR and DDR2 DIMMs.

Type	Name	Bus speed	DDR transfers	Peak throughput
DDR	PC1600 (PC200)	100 MHz	200 MHz	1.6 GBps
DDR	PC2100 (PC266)	133 MHz	266 MHz	2.1 GBps
DDR	PC2700 (PC333)	167 MHz	333 MHz	2.7 GBps
DDR	PC3200 (PC400)	200 MHz	400 MHz	3.2 GBps
DDR2	PC2-3200	200 MHz	400 MHz	3.2 GBps
DDR2	PC2-4300	266 MHz	533 MHz	4.3 GBps
DDR2	PC2-5300	333 MHz	666 MHz	5.2 GBps

More detailed SDRAM specification information can be found at http://developer.intel.com/technology/memory/

As shown in the figure above, when comparing DDR and DDR2 at the same external frequency (400 MHz dual-edge), the throughput is the same. In addition, due to the internal core frequency of DDR2 being half that of DDR, there is more scope to increase frequencies and therefore increase the bandwidth of DDR2. However, the lower memory core frequency means longer latency time, the time it takes to set up the request for data transfer.

The end result of this is that at DDR2 lower frequency of 400 MHz, which is the DDR upper frequency, the two technologies offer equal throughput but DDR2's latency is worse. However, as DDR2 increases in frequency (DDR has practically reached its limit), throughput will increase and latencies will equalize.

Related product families

Product families related to this document are the following:

- Memory

Notices

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